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Cross-Current SOI MOSFET and Application to Multiple Voltage Reference Circuits

Yasuhisa Omura**, Yoshio Mimura** and Masakazu Kitagawa**

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Abstract

This paper introduces important aspects of the cross-current tetrode (XCT) SOI MOSFET and proposes its application to practical multiple-voltage-reference supplier circuits. Important functions of the proposed circuits are simulated on the basis of measured device characteristics.

I. Introduction

One of the authors (Omura) proposed the cross-current tetrode SOI MOSFET (XCT-SOI MOSFET) and examined analog applications (see Fig. 1). Though the scaling feasibility of XCT-like devices has been studied recently, we think XCT devices will yield new applications such as high-voltage devices and SRAM memory cells with high noise margin. In order to assess those applications in sufficient detail, device models are needed to perform circuit simulations. Since Y. Azuma et al. has recently proposed an advanced device model for the XCT MOSFET, we are now able to study device applications.

This paper proposes switched multiple-reference-voltage supplier circuits for low-power SOI LSIs. We examine their functions by circuit simulations (SPICE) on the basis of measured XCT MOSFET parameters. The usefulness of the XCT SOI MOSFET is demonstrated.

II. Device Structure and Assumptions for Simulations

A. Device structure and features

Schematic device structure is shown in Fig. 1. In an XCT device, the n-channel MOSFET and p-channel JFET are self-merged and the electron current of the nMOSFET is relayed to the hole current of pJFET in series. The XCT device offers negative differential conductance in the saturation region of drain current, as shown in Fig. 2. Device parameters of fabricated devices are summarized in Table 1. In Fig. 2, symbols show results yielded by the device model proposed by Azuma et al. Since the XTC device has active body contact, the body-floating effect is automatically eliminated.

B. Assumptions for simulations

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Fig. 1  XCT SOI MOSFET (plan and cross-sectional views)
(a) Plan view of XCT device.
(b) Cross-sectional view of device along MOSFET channel.
(c) Cross-sectional view of device along a-a’ and b-b’.

Fig. 2  $I_D-V_D$ characteristics of XCT device Calculation results (symbols) are also shown for comparison$^b$. 
Fig. 3  Equivalent circuit model for a nXCT device and an XCT CMOS device.
(a) Fundamental equivalent circuit
(b) CMOS circuit composed of nXCT and pXCT devices

Table 1. Physical parameters of fabricated devices.

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<th>Device parameters</th>
<th>Values [units]</th>
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<tr>
<td>Nominal body doping, (N_i)</td>
<td>(1 \times 10^{16} \text{ cm}^{-2})</td>
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<tr>
<td>Gate width, (W_n/W_p)</td>
<td>10/20 [(\mu\text{m})]</td>
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<tr>
<td>Gate length, (L)</td>
<td>2 [(\mu\text{m})]</td>
</tr>
<tr>
<td>Gate oxide thickness, (t_{ox})</td>
<td>30 [(\mu\text{m})]</td>
</tr>
<tr>
<td>SOI layer thickness, (t_{SOI})</td>
<td>350 [(\mu\text{m})]</td>
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In circuit simulations, we assume the equivalent circuit for the nXCT device as shown in Fig. 3(a). We examined if the equivalent circuit reproduced the I-V characteristics of the XCT device. We determined the SPICE simulation parameters using the device parameters shown in Table 1.

III. Proposal of Voltage Reference Circuits and simulation Results

A. Two Reference Voltage Circuits

We first propose a two-reference-voltage circuit, each with one XCT CMOS device. In Fig. 3(b) the XCT devices are shown as equivalent circuits. This is a simple CMOS configuration except for the independent gate terminals of the nXCT device and the pXCT devices. It is assumed that \(V_{DD} = 5\) V and the gate voltage of pXCT device \((V_{GP})\) holds a constant value. Threshold voltages are \(+0.6\) V for nXCT and \(-0.6\) V for pXCT.

The concept of switching the reference voltage is shown in Fig. 4, where simulated time
sequences of the gate voltage of the nXCT device ($V_{GN}$), output voltage ($V_{out}$) and $V_{DD}$ are shown. Switching mechanisms are schematically shown in Fig. 5, where the four figures correspond to notations 'a' to 'd' in the time evolution shown in Fig. 4.

At $V_{DD}$ = 0 V and $V_{GN}$ = 3 V, $V_{GN}$ first rises from 0 V to 2 V. When $V_{DD}$ rises from 0 V to 5 V (it takes several microseconds), the $V_{out}$ level rises from 0 V to 1 V ($V_L$), where $V_L$ represents the target reference voltage. This process is shown in Fig. 5(a). Next, At $V_{DD}$ = 5 V, $V_{GN}$ falls to 0 V and $V_{out}$ rises to 5 V. This process is shown in Fig. 5(b). After that, $V_{GN}$ rises from 0 V to 2 V again, which leads $V_{out}$ to the other target reference voltage ($V_h$); in this case, $V_h$ = 4 V.
This process is shown in Fig. 5(c). When $V_{CP}$ falls to 0 V in this stage, $V_{out}$ also falls to almost 0 V, as shown in Fig. 5(d).

We note that the sequence shown in Fig. 4 is quite inconvenient. Our solution is to propose a more practical control method. Fig. 6 shows the example of switching $V_{out}$ ($V_L \rightarrow V_H$). In the operation shown in Fig. 6, a falling trigger is applied to $V_{CP}$ and a rising trigger is applied to $V_{GN}$. At the initial stage, $V_{DD}$ of 5 V is applied to the circuit, whereupon $V_{GN}$ rises to 2 V, and finally $V_{CP}$ rises to 3 V; so, $V_{out}$ holds $V_L$ level at the initial stage. In Fig. 6, at $t = 0.4$ μsec, $V_{CP}$ steps down by 0.8 V for a short time and then rebounds, followed by a high $V_{out}$ level ($V_{ph}$); this process is illustrated in Figs. 7(a) and 7(b). The locus of the cross point of current
curves of nXCT and pXCT devices moves from \( V_L \) to a higher level following the sequence shown in Fig. 7(a), and it finally returns to \( V_H \) when \( V_{GP} \) returns to 3V, as shown in Fig. 7(b). At the next stage, \( V_{CN} \) rises by 0.8 V at \( t=0.8 \) µsec and returns to 2 V; this trigger forces \( V_{out} \) to step down to \( V_L \). This sequence is illustrated in Figs. 7(c) and 7(d).

B. Three Reference Voltage Circuits

We also propose a three-reference-voltage circuit for practical convenience: its circuit diagram is illustrated in Fig. 8. The circuit is composed of two XCT CMOS devices that are connected sequentially. Time evolution of signals (\( V_{xin} \) and \( V_{xip} \)) and \( V_{out} \) is shown in Fig. 9. The basic operation mechanisms are the same as those illustrated in Fig. 7.

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**Fig. 8** Three reference-voltage circuit.

**Fig. 9** Time evolution of \( V_{xin}, V_{xip}, \) and \( V_{out} \).
Thus, multiple reference-voltage circuits can easily be realized with XCT CMOS devices as described above. Since the through-current of the XCT CMOS is very low [3, 4], power dissipation of the proposed circuits is quite low. These considerations strongly suggest that the XCT CMOS is promising for use as a key devices for future SOI LSIs.

IV. Summary

This paper introduced important aspects of the cross-current tetrode (XCT) SOI MOSFET and proposed its application to practical multiple reference-voltage suppliers. Fundamental functions of the proposed reference-voltage supplier circuits were examined by circuit simulations (SPICE) on the basis of measured XCT MOSFET parameters. The usefulness of XCT SOI MOSFETs was demonstrated.

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References